FINFET CMOS WITH NVRAM CAPABILITY

Abstract of the Disclosure

The present invention provides a device design and method for forming the same that results in Fin Field Effect Transistors having Non-Volatile Random Access Memory (NVRAM) capability. NVRAM capability arises from the presence of double floating gates arranged on and insulated from a semiconductor fin body, and a control gate arranged on and insulated from the double floating gates. The fabrication of the present device may be accomplished by: providing an SOI wafer and defining a fin on the SOI wafer, the fin may be capped with an insulator layer; providing gate insulator on at least one vertical surface of the FIN; depositing floating gate material over the gate insulator; depositing insulator material on the floating gate material to form the floating gate isolation; depositing control gate material over the isolated floating gate material; removing a portion of the control gate material to expose source and drain regions of the Fin, implanting the Fin to form source/drain regions in the exposed regions of the Fin, and providing insulator material on the Fin. In addition, the NVRAM FinFET allows for horizontal current flow.